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Final Report on the Transformational Manufacturing Technology Initiative (TMTI) ManTech Research Project S1057: Tin Whisker Mitigation

The Use of Robotic Solder Dipping to Replace Electronic Part Surfaces Finishes of Pure Tin With a Tin-Lead Finish

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The Use of Robotic Solder Dipping to Replace Electronic Part Surfaces Finishes of Pure Tin with a Tin-Lead Finish

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EXECUTIVE SUMMARY

The goal of the Robotic Solder Dip Project was to qualify a number of electronic component package types for reprocessing from pure tin (Sn) termination finishes to tin-lead (Sn-Pb) by employing a slightly tailored, commercially available robotic process in which a whisker-prone pure tin finish is completely removed from component leads and replaced by a 'whisker-safe' tin-lead finish without damaging the part. To accomplish this, a team of experts selected the package types to be used in project, favoring those commonly used in high reliability designs. For each package type, a representative part was selected for robotic solder dip testing. An additional criterion in part selection was to focus on those that were expected, based on the team's failure mode expertise as well as past history by the commercial vendor, to pass all tests before and after solder dipping. A number of high reliability programs were literally waiting to use the results of this qualification test, so the maximum number of successes was desired.

The selected parts were subjected to a rigorous series of pre-dip electrical and environmental tests to ensure that they were 'good' parts. They were then robotically solder dipped by the commercial vendor using the vendor's normal process, which was slightly tailored to reduce the potential for thermal damage to the parts. The parts were subsequently retested and a number were subjected to destructive physical analysis (DPA) to look for damage, if any, resulting from the dipping process.

This report describes the research conducted and provides necessary information for any program wishing to employ the documented robotic solder dip process, whether performed in-house or through services provided by a vendor possessing the requisite equipment and expertise, as a means of preventing tin whisker growth on the types of parts addressed in the report. Although a limited budget precluded selection of as many parts as would have been desirable, almost all of the selected part types were successfully solder dipped and passed all testing, providing program managers and product designers a means of mitigating the reliability risk posed by tin whiskers on a wide variety of component package types.

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1. INTRODUCTION

1.1 PURPOSE

The goal of the TMTI Robotic Solder Dip Project was to provide one means of partially mitigating the reliability threat posed by tin whiskers by qualifying a number of electronic components package types for reprocessing using a tailored, commercially available, robotic solder-dip process. The process replaces a whisker-prone pure tin (Sn) termination finish with a tin-lead (Sn-Pb) finish. This report provides the rationale for conducting the Project, a detailed description of the tests conducted and their results as well as the process controls and other information needed by anyone desiring to employ the robotic solder process on parts qualified by the tests. For brevity, the TMTI Robotic Solder Dip Project will be referred to herein as 'the TMTI Project' or simply 'the Project.'

1.2 BACKGROUND

A failure mechanism affecting electronic parts as well as some mechanical parts is re-emerging that has previously been responsible for degradation of mission readiness and an estimated loss of at least a billion dollars worth of satellites, military-aerospace and other equipment — electrically conductive 'tin whiskers'. Tin whiskers can develop under typical operating conditions on any product type that uses lead-free pure tin coatings. Driven by the worldwide accelerating movement to lead-free products, part manufacturers are transitioning to lead-free products at a rapid rate. The lead-free part finish of choice is predominantly pure tin, and products that use it will be susceptible to tin whisker growth. Tin whiskers pose major safety, reliability and potential liability threats to all makers and users of high performance and/or high reliability electronics and associated hardware. Increasing dependence on COTS parts and assemblies renders military-aerospace-medical and other high reliability original equipment manufacturers (OEM) and the programs they support particularly vulnerable to whisker failures. Existing approaches are not sufficient to prevent or control whisker growth. The risk is here now. Even if such contractors are exempt from lead-free legislative requirements, this is of little or no value if the commercial electronic part manufacturers on which they increasingly depend convert to solely lead-free product lines.

When Corfin Industries demonstrated to Raytheon in the fall of 2002 a process they claimed could completely replace 100% of the tin plate on fine-pitched microcircuits without solder bridging, some members of the CALCE Tin Whisker Group asked what kind of damage, if any, happens inside the microcircuit during the dip. The consensus was that there are numerous unknowns and that it would be helpful to many defense programs if the answer is known. A TMTI Robotic Solder Dip was proposed to ONR to provide the answer and hopefully qualify a variety of existing part package styles on their ability to survive the thermal shock involved with the existing solder dip process. The process requires that both the part's leads as well as part of the part's body be immersed in molten solder. Based on their "physics-of- failure" experience, the investigators at CALCE considered the thermal shock on the part to be a potential cause of fracture of a bond wire (immediate failure) or a fracture of the encapsulant bond at the corners of the microcircuit's die. The occurrence of the latter could initiate a series of related failure mechanisms that would result in a field failure several years after the solder dip. Therefore,

qualification of parts for using the robotic solder-dip process require that a statistically significant environmental life test be performed to verify the existence or lack of failure modes resulting from the solder dip on each part package style.

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2. ROBOTIC SOLDER DIP PROJECT OVERVIEW

As previously stated, the goal of the TMTI Robotic Solder Dip Project was to qualify a number of electronic components for reprocessing using a tailored, commercially available robotic solder-dip process. A team of experts selected the package types and representative parts to be used in project, favoring those commonly used in military-aerospace and other high reliability designs. An additional criterion in part selection was to focus on those parts that were expected to pass all tests before and after solder dipping, based on the team's failure mode expertise as well as past history by the commercial vendor. The parts were tested, robotically solder dipped, tested again, and destructively analyzed. This report documents the processes and tests employed in the project and the results achieved. Together, they constitute guidelines that can be used by any company or program as a baseline for developing their own robotic solder dip process. The Office of Naval Research (ONR) Manufacturing Technology (ManTech) Program funded this project. Its description may be viewed on the ONR Web site (www.onr.navy.mil) as S1057 Tin Whisker Mitigation in the FY2006 Project Book. Key performers on the project included the Navy Best Manufacturing Practices Center of Excellence, College Park, Maryland; Raytheon Missile Systems (RMS), Tucson, Arizona; Raytheon Integrated Defense Systems (IDS), Tewksbury, Massachusetts; the Computer-Aided Life Cycle (CALCE) Electronic Systems and Products Center (ESPC) at the University of Maryland, College Park; and Corfin Industries LLC, Salem, New Hampshire. Additional technical review was received from the CALCE Tin Whisker Group, an ad hoc group with members of government, industry, and academia and more than 85 sites involved. This group has weekly telephone conferences, multiple collaborative projects, and a common focus on finding solutions to mitigate the risk of tin whiskers that grow on pure tin-plated parts. This group is primarily motivated by the need to meet the mission assurance requirements for high reliability military-aerospace projects. The performers for the Robotic Solder Dip Project are all core members of the CALCE Tin Whisker Group.

The project was structured as follows, and includes core team members assembled with the following allocated responsibilities:

- NAVY BMPCOE: Government-side project management and communication, Collaborative Work Environment (CWE)
- Raytheon Tucson: Contractor-side project management, coordination and communication
- Raytheon Tewksbury: Test direction and performance
- CALCE Electronic Products and System Center (EPSC) at the University of Maryland: Part subject matter experts, failure analysis
- Corfin Industries: Robotic solder dip

The core team evolved a test plan with a goal of testing as many package styles as it could that would be used on high reliability programs given the budget and time constraints of the contract. A large number of candidate package styles were identified, followed by the substantial effort of choosing actual parts to be used in the test. This involved the core team plus reviews by various members of the CALCE Tin Whisker Group and various Navy programs at Raytheon. The core team applied various filters to the part selection, including moisture sensitivity levels, die technology, cost and availability of part, cost to functionally test the part, market maturity, etc. Parts were then ordered, with some parts obtained through a cancelled Navy program. Testing of

the parts involved functional testing and scanning acoustic microscopy inspection of the parts both before and after the robotic solder dip. This was followed by environmental stress testing designed to expose any failure modes caused by the solder dip, and then by more functional testing, acoustic microscopy, and finally destructive physical analysis. The goal of the test was then to determine if the robotic solder dip process caused any damage to any part for each package style that was tested.

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3. APPROACH

Since the TMTI Robotic Solder Dip involves immersing the full length of the leads and the edge of the package into molten eutectic tin-lead solder at 245ºC, the package will be subjected to more thermal shock than would normally be the case for preparing the leads for soldering to the circuit board (preconditioning). The use of this report is predicated on making use of the TMTI test results as well as existing practices for part use. A basic rule of thumb for building reliable circuit boards with microcircuits —"Start with good parts, and then don't damage them." —is quite applicable in the following sub-sections.

The solder dip process examined in this study involved the use of a eutectic tin-lead alloy only. Other alloys may be proposed for use for solder dip application in the future, including lead-free SAC alloy (tin-silver-copper), tin-bismuth, tin-copper, or other compositions. The use of different alloys may result in different thermal stresses induced in the parts and may not provide the same level of tin whisker risk mitigation as with eutectic tin-lead. The results of this study should not be used to draw either positive or negative conclusions regarding the suitability of any alloy other than eutectic tin-lead for use in solder dipping of components.

Utilize effective part selection method to ensure incoming quality

Robotic solder dipping is a post-processing technique for commercially available electronic parts that is not endorsed by the part manufacturers. For this reason, it is likely that part manufacturers will not accept responsibility or even be cooperative in investigating the failures of parts that have gone through the solder dipping process. It is necessary that the engineering process used to select the parts to go through the robotic solder dipping process be thorough and well documented. An industrially accepted part selection and management guideline such as the one developed by the CALCE Center (Parts Selection and Management, Pecht, Michael G., Editor, John Wiley & Sons, Inc., 2004) should be used for selecting the parts that are to be used in solder dipping.

Utilization of a robust parts selection and management process will ensure that high quality part lots are used for robotic solder dip (and even when not doing a robotic solder dip). Ideally, the robotic solder dip process should merely replace the termination finish without any other deleterious effect on the part. However, when a part with quality problems is used for solder dipping, those problems will remain through the dipping process and could be exacerbated by it. In many cases, initial quality problems can have other effects too. For example, already oxidized leads may not be properly finished after dipping. Delamination in plastic encapsulated microcircuits (PEMs) between the encapsulating epoxy and the part's die surface is the precursor of corrosion failure modes that occur in the field. Microcircuits that are inadvertently purchased with delaminations may experience a slight increase in the delamination area after the robotic solder dip and a substantial increase when deployed to the field in a harsh environment. Although many microcircuits will survive with small delaminations, the cumulative stress from all sources, particularly those from deployment to a harsh environment, is not a desired scenario for a long service-life. To ensure that purchased parts are free of problematic delaminations, they should be sample checked. One method is to use a Scanning Acoustic Microscope (SAM). (If SAM is employed, areas of concern are those over the top of the die. Small delaminations in the corner of the die can demonstrate substantial growth when subjected to substantial environmental stress. This was the case with an Altera 208-pin quad flat pack used in the Project

test. It had minor delaminations prior to the start of the test. However, these became major delaminations after the environmental life test, and that was independent of whether or not the part had been robotically solder dipped. A variation of that same quad flat pack with no initial delaminations experienced no delaminations from the solder dip or the environmental life test. JEDEC J-STD-020C document on PEMs also contains useful criteria for evaluation of delamination. In any case, particularly if sample checking will not be employed, and to the extent possible, parts should be purchased from companies with major product lines because their process control is usually sufficient to continually provide good products.

In the absence of appropriate part selection and management methods, incoming inspection of parts is strongly recommended. The inspection should focus on lead cleanliness and the quality of initial plating and on the possible presence of interfacial delamination. If high reliability is a preeminent requirement (i.e., whisker failures are unacceptable), the use of X-ray fluorescence (XRF) equipment to confirm that component lead plating is not pure tin is recommended.

3.1 Considerations for Parts Being Drawn from Long-Term Storage

If the parts to be solder dipped must be drawn from long-term storage, the original quality ensured through the part selection and management may no longer be valid. It is necessary to obtain and accurately record the conditions in which the parts were stored. In particular, the thermal, humidity and corrosive gas conditions need to be recorded. It will also be necessary to perform inspection of the leads and evaluations for possible presence of interfacial delamination.

3.2 Perform a Bake-Out on All Parts Prior to Solder Dip

All parts selected for solder dipping should be baked out at the temperature/time combination specified in J-STD-033B depending on the moisture sensitivity level (MSL) of the part. However, for uniform process flow independent of the part MSL, one may choose to bake at a time/temperature combination of the highest (i.e., worst) MSL (currently 5a) part based on the part thickness. For parts with unknown MSL, the bake-out should be carried out at the worst-case level.

4. TEST RESULTS AND APPLICATIONS

This section provides a summary of the parts evaluated, observations regarding those that passed testing and the one that did not, guidelines for 'qualification by similarity' for parts not included in the testing, and a discussion of additional part types not covered in the study.

4.1 TABULAR SUMMARY OF PARTS EVALUATED

The tables below summarize the representative parts from the 23 package types that were evaluated to confirm (or not confirm) that they can be successfully robotically solder dipped without damage to the part. The tables do not show all variables used in package selection.

Table 4-1: Description of parts that passed the solder-dip qualification test

Package Type	Representative Part outline	Part Number and Manufacturer	Part function	MSL Level (for PEMs only)
14-pin Plastic DIP (plastic dual inline package), through-hole, coarse pitch, copper lead frame		SN74HC00N Fairchild	NAND function high speed CMOS device	Thru-hole part, not MSL rated
16-pin Plastic TSSOP, (thin-shrink small outline package) surface mount, coarse pitch, copper lead frame		ADG608TRU Analog Devices	CMOS Analog Multiplexers	1
32-pin Plastic TQFP (thin quad flat pack), surface mount, coarse pitch, copper lead frame		IDT72V11081 IDT	CMOS SYNCFIFO	3

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Package Type	Representative Part outline	Part Number and Manufacturer	Part function	MSL Level (for PEMs only)
3-pin Plastic TO-92 (transistor package), through-hole; coarse pitch, copper lead frame	1 2 3	2N3906 On-Semi	General purpose PNP transistor	1
3-pin Plastic TO-220, through-hole, copper lead frame	G D S TO-220F FQPF Series	FQPF47P06 Fairchild	MosFET power transistor	Thru-hole part, not MSL rated
3-pin Plastic SOT 23, surface mount, coarse pitch, alloy 42 leadframe with copper underplating	3 1 2	MMBT2222ALT1 On-Semi	Bipolar transistor	1
14-pin Plastic SOP (small outline package), surface mount, coarse pitch, copper lead frame was nickel-plated		74AC14SC Fairchild	Hex inverter with Schmitt trigger input	1
8-pin Plastic SOIC, surface mount, coarse pitch, copper lead frame	8 5 1 4	OP284ES Analog Devices	Operational amplifier	1
plastic SOIC, surface mount, coarse pitch, copper lead frame		IDT720415SOI IDT	CMOS ASYNC FIFO	3

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Package Type	Representative Part outline	Part Number and Manufacturer	Part function	MSL Level (for PEMs only)
2-pin Plastic SOD-123, surface mount, alloy 42 leads		1N4148W-7 Diodes Inc	Diode	1
8-pin Plastic SOP, surface mount, coarse pitch, copper lead frame		SI4967DY Siliconix	Transistor	1
208-pin Plastic QFP (quad flat pack), surface mount, fine pitch, copper lead frame	ALTERA	EPM7256AQC208-7 Altera (Max family)	Erasable PLD	3
208-pin Plastic power QFP (quad flat pack), heat spreader, surface mount, fine pitch, copper lead frame	ALTERA	EPM7256SRC208-7 Altera (Max family)	Erasable PLD	3
20-pin Plastic PDIP (plastic dual in-line package), through-hole, coarse pitch, copper lead frame		MM74HC540N Fairchild	Inverting octal 3-state buffer	Thru-hole part, not MSL rated
28-pin Plastic LCC (leaded chip carrier), surface mount, coarse pitch, copper lead frame		DAC8412FPC Analog Devices	Quad DAC	5

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Package Type	Representative Part outline	Part Number and Manufacturer	Part function	MSL Level (for PEMs only)
32-pin Plastic LCC (leaded chip carrier), surface mount, fine pitch, copper lead frame		IDT7201LA12J IDT	FIFO dual port memory	1
20-pin ceramic LCC (leadless chip carrier), surface mount, coarse pitch, lead frame material yet to be determined		54ACT00LMQB Fairchild	Quad NAND Gate	NA
16-pin CERDIP (ceramic dual in-line package), through hole, coarse pitch, alloy 42 lead frame		AM26LS31DC TI	Quad differential. line receiver	NA
16-pin CERDIP (ceramic dual in-line package), through-hole, coarse pitch, alloy 42 lead frame		DS26LS32MJ National Semiconductor	Quad differential line receiver.	NA
14-pin CERDIP (ceramic dual in-line package), through-hole, coarse pitch, alloy 42 lead frame		LT1058MJ/883B Linear Tech	Quad operational amplifier	NA
14-pin CERDIP (ceramic dual in-line package), through-hole, coarse pitch, alloy 42 lead frame		OP490AY Analog Devices	Quad operational amplifier	NA
16-pin CERDIP (ceramic dual in-line package), through-hole, coarse pitch, alloy 42 lead frame		SN75ALS195J TI	Quad differential line receiver	NA

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Table 4-2: Description of parts that did not pass the solder-dip qualification test

Package Type	Representative Part outline	Part Number and Manufacturer	Part function	MSL Level (for PEMs only)
100-pin, Plastic TQFP (thin quad flat pack), surface mount, fine pitch, copper lead frame		EPM7128STI100-10 Altera	Erasable PLD	3

4.2 USING PROJECT DATA TO QUALIFY COMPONENTS FOR SOLDER DIPPING

Each of the 22 parts listed in Table 4-1 that successfully passed all the testing is considered to be fully qualified for processing by robotic solder dip in accordance with the process parameters described herein. Parts different from the 22 listed must be qualified in some manner to be considered suitable candidates for robotic solder dip. Section 4.3 provides information and process parameters for determining whether a part is, or is not, eligible through “Qualification by Similarity.” Parts that do not meet the criteria should be qualified through additional testing. Whether or not such parts would need to undergo testing that is the same or equivalent to that performed on the TMTI parts is an engineering decision. Factors that should be considered when determining appropriate qualification testing and analysis include: vulnerability of the component to thermo-mechanical damage, relevant reliability history, environmental stresses induced during manufacturing, test, storage, transportation, and field usage, among other factors.

4.3 QUALIFICATION BY SIMILARITY: A GUIDELINE FOR DETERMINING IF PARTS SIMILAR TO THE TEST PARTS WILL SURVIVE THE TMTI SOLDER DIP WITHOUT DAMAGE

All of the detailed results from the testing and evaluation of the components in this study were reviewed to identify when and why certain components are vulnerable to thermal-mechanical damage. This section describes how those results were used to develop a simple metric for use in determining whether or not a particular component may be considered as a candidate for qualification by similarity to another previously qualified component. An example is provided at the end of this section illustrating use of the metric in a hypothetical situation.

4.3.1 Package and die geometry characterization

Table 4-3 provides package and die dimensions for all 23 part types, which were obtained from X-ray images for each. Further, the ratio of die area to package thickness was calculated in each case to provide a single factor which could be used to analyze the combined effect of die area and package thickness on the possibility of thermo-mechanical damage due to dipping. Part types 3, 8, 11, and 15 showed a propensity for thermo-mechanical damage. While the observed

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delamination for part type 3 was only marginal and deemed insignificant, additional mini-tests run in the project confirmed that the anomalies for part types 8 and 15 were not attributable to solder dipping but were a result of the environmental exposure subsequent to dipping. Part type 11 was, however, identified as having the highest risk of thermo-mechanical damage from dipping. This was also the only part type among those tested to not be qualified for solder dipping.

Table 4-3: Package and die geometry characterization data

Identifier	Package configuration	Part type	Pin count	Pitch (mm)	Package dimensions			Die dimensions			Ratio of die-area to package thickness (mm)
					Length (mm)	Width (mm)	Thickness (mm)	Length (mm)	Width (mm)	Thickness (mm)	
1	Small Outline Packages	SOP	8	1.27	5.2	4.1	1.6	2.5	1.9	0.3	2.97
2		SOP	14	1.27	8.7	4.0	1.8	2.0	0.9	0.4	1.00
3		TSSOP	16	0.65	5.1	4.5	1.0	2.4	1.6	0.4	3.84
4		SOIC	8	1.27	5.0	4.0	1.6	2.8	2.1	0.3	3.68
5		SOIC	28	1.27	18.5	8.9	2.7	3.2	0.8	0.5	0.95
6	SOD/SOT	SOT-23	3	2.00	3.0	1.4	1.1	0.5	0.4	0.4	0.18
7		SOD-123	2	NA	2.9	1.7	1.4	0.3	0.3	0.4	0.06
8	Plastic Quad Flat Packs	PQFP	208	0.5	28.1	28.1	3.6	7.9	4.8	0.4	10.53
9		PQFP	208	0.5	28.1	28.1	3.6	6.7	5.1	0.5	9.49
10		PQFP	32	0.8	7.0	7.0	1.5	2.2	1.8	0.3	2.64
11		TQFP	100	0.5	14.5	14.5	1.1	4.8	4.8	0.3	20.95
12	Plastic Leaded Chip Carriers	PLCC	28	1.27	11.6	11.6	3.9	5.8	4.6	0.5	6.84
13		PLCC	32	0.8	14.1	11.5	1.7	2.5	2.0	0.5	2.94
14	Plastic TO	Plastic TO-92	3	1.4	5.3	5.2	4.2	0.3	0.3	0.2	0.02
15		Plastic TO-220	3	2.54	16.1	10.4	4.9	6.0	6.3	0.3	7.71

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Identifier	Package configuration	Part type	Pin count	Pitch (mm)	Package dimensions			Die dimensions			Ratio of die-area to package thickness (mm)
					Length (mm)	Width (mm)	Thickness (mm)	Length (mm)	Width (mm)	Thickness (mm)	
16	Plastic Dual –In-Line-Packages	PDIP	14	2.54	19.6	6.6	3.6	1.6	0.9	0.3	0.40
17		PDIP	20	2.54	26.4	6.7	3.4	2.4	1.5	0.2	1.06
18	Leadless Ceramic Chip Carrier	LCCC	20	1.27	8.9	8.9	1.9	1.1	1.1	0.5	0.64
19	Ceramic Dual-Inline Packages	CERDIP	16	2.54	19.9	7.9	3.6	1.8	1.8	0.5	0.90
20		CERDIP	16	2.54	19.9	7.9	3.6	2.0	1.7	0.4	0.94
21		CERDIP	14	2.54	19.9	7.9	3.6	2.7	2.0	0.5	1.50
22		CERDIP	14	2.54	19.9	7.9	3.6	3.8	3.3	0.4	3.48
23		CERDIP	16	2.54	21.3	7.6	3.6	2.3	2.0	0.3	1.28

4.3.2 Discussion of results from die and package geometry characterization

When the ratio of die area to package thickness was plotted against each of the part types indicated in Figure 4-1, the Plastic Quad Flat Packs (PQFP) (part types 8, 9 and 11) were found to have the largest values of this ratio. It was also found that the part types 3, 8, 11 and 15 that had shown anomalous behavior (and thus, possible propensity to thermo-mechanical damage) also had the largest ratios among other part types of similar package configuration. For example, the 16-pin TSSOP (part type 3) had the largest ratio among all small surface-mount part types (SOP/SOIC/SOT/SOD). Similarly, the 208-pin PQFP (part type 8) and 100-pin TQFP (part type 11) had the largest value among all PQFPs. Again, the 3-pin TO-220 (part type 15) had the larger value of this ratio between the two plastic TO part types used in the study.

It may be noted that the 3-pin SOT 23 (part type 6), 2-pin SOD 123 (part type 7) and the 3-pin TO-92 (part type 14) had particularly small die, with die dimensions less than or equal to 500 µm in each case. Conversely, the 8-pin SOIC (part type 4) and 28-pin PLCC (part type 12) had reasonably large die sizes as compared to the corresponding package size. In each of these part types, no anomalies (possibly due to thermo-mechanical damage) were observed.

Figure 4-1: Ratios of die area to package thickness for each part type showing the number of parts that had anomalous behavior for the relevant part types

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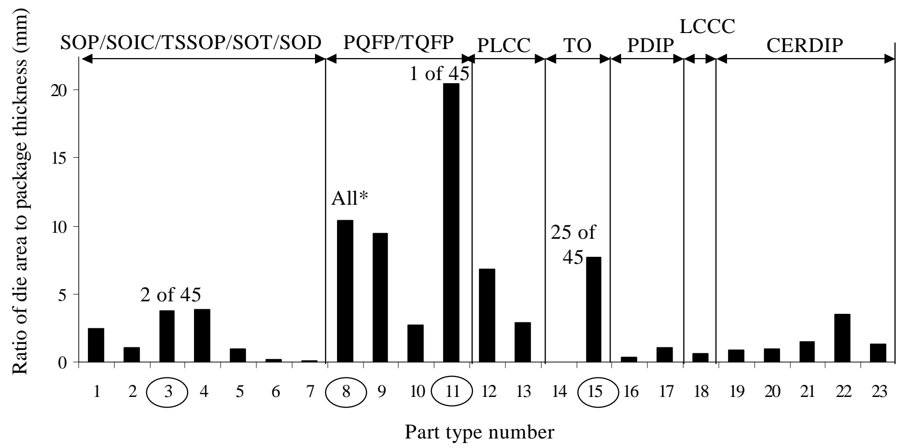

4.3.3 GUIDELINES FOR ADDITIONAL PART TYPES NOT COVERED IN THE SCOPE OF THIS STUDY

All part types that did not show any anomalous behavior (i.e., those attributable to possible thermo-mechanical damage from solder dipping) were grouped as per package configuration. Part types 8 and 15, which had shown evidence of thermo-mechanical damage due to environmental exposure and not because of solder dipping, were also included in this grouping. Maximum and minimum ratios of die area to package thickness were plotted for each package configuration as indicated in Figure 4-2. This can be used before solder dipping part types not explicitly described by any of the 23 part types provided in

Table 4-3 to assess the possibility of thermo-mechanical damage. The electronic part user should X-ray part types to obtain die and package dimensions and calculate the die area to package thickness ratio. This value can be compared with the ratios indicated in Figure 4-2 for the appropriate package configuration.

For any ratio that lies in the range between the minimum and maximum values shown in Figure 4-2, the part type is not expected to suffer from any thermo-mechanical damage due to dipping, as this ratio is within the range of values for part types covered in the study that did not show any evidence of such damage. If the ratio is below the minimum value, no thermo-mechanical damage is expected as before. However, it must be made clear that this study did not qualify part types with ratios lower than the minimum values indicated in Figure 4-2.

A caveat needs to be applied for part types, where the ratio of die-area to package thickness exceeds the maximum value indicated. For PQFP and TO package configurations, the maximum value may be further extended up to the value for those part types (8 and 15) that showed thermo-mechanical damage due to the environmental exposure and not because of solder dipping, as indicated in the figure. However, user discretion may be recommended in such cases, as these part types did indicate propensity for thermo-mechanical damage.

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For all package configurations, when part types exceed limits of values, as indicated in the bars in Figure 4-2, additional studies and/or tests will be required on part types to ascertain whether these would be prone to any thermo-mechanical damage due to dipping. The analysis should be as extensive as the ones carried out for the parts in this study.

As an example of "Qualification by Similarity," consider a Quad Amplifier manufactured by Analog Devices in a 64 pin Plastic LCC (PLCC-64) package (part number AD8335ACPZ). Package thickness is given in the Analog Devices Data Book as 0.65 (typical) to 0.80 (max) millimeters. The die dimensions were not given in the data book. They were determined by X-ray, and reported by the lab to be .139 by .142 inches, for a die area of .0197 square inches. There is a caution here on calculating the ratio of die area to package thickness: do not forget that this ratio has a dimension. To be consistent with Table 4.3 the die dimensions must be converted to millimeters: 0.139 * 25.4 = 3.53 mm by 0.142 * 25.4 = 3.61 mm. The resultant die area is 12.7 square millimeters. This gives a range of the ratio of die area to package thickness of 15.9mm to 19.6mm. Compare this to the PLCCs tested in TMTI shown in Table 4.3. The PLCC-28 had a ratio of 6.81, and the PLCC-32 had a ratio of 2.87. Remember, the larger the ratio, the greater the susceptibility of the package to thermo-mechanical damage. The (example) PLCC-64 has a much larger ratio of die area to package thickness than either of the test parts, and is therefore NOT qualified by similarity as a candidate for the TMTI Robotic Solder Dip. What does this mean? It means that the TMTI test data is insufficient to allow an extrapolation of qualification for that package. If a TMTI solder dip is done on that package it may or may not suffer any thermo-mechanical damage. Nevertheless, for a desperate user of the PLCC-64 package that decides to try a solder dip, use of the TMTI process would likely give the greatest chance for success (as opposed to other solder dip techniques). The temperature parameters chosen for TMTI were a trade-off between minimizing the chance of thermo-mechanical damage and the necessity of still being able to achieve adequate solder wetting for complete replacement of the pure tin.

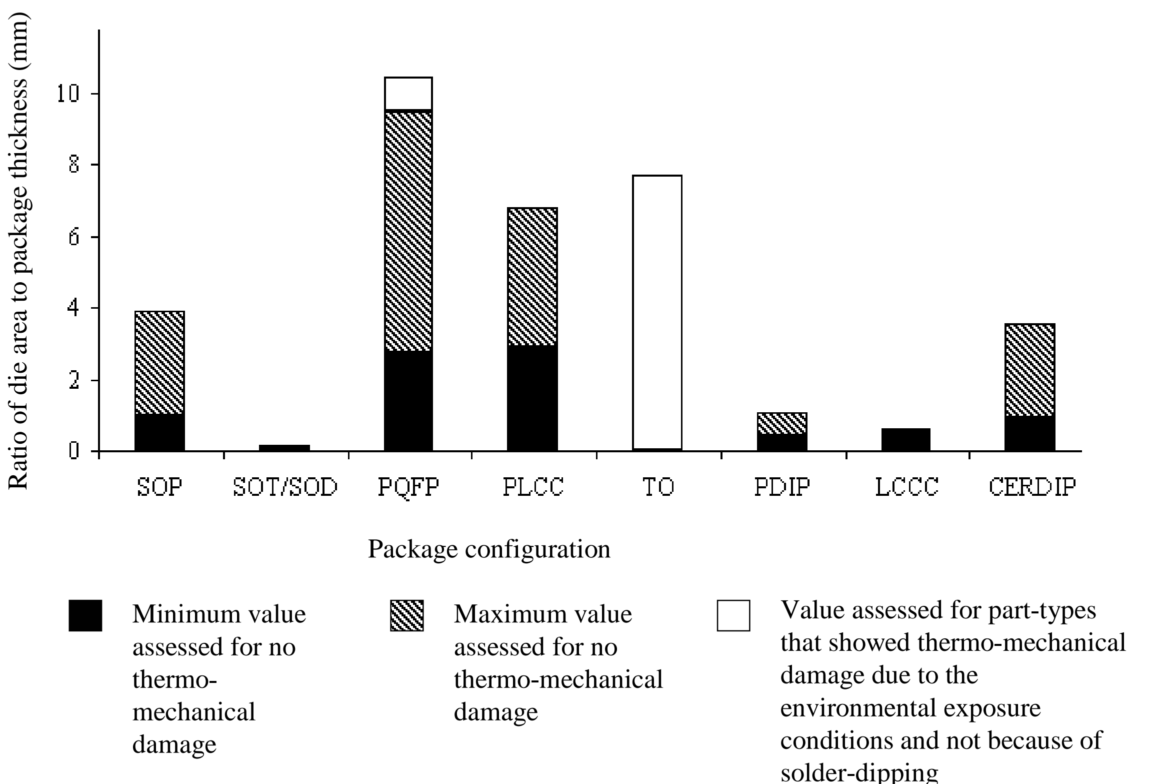

Figure 4-2: Ratios of die-area to package thickness of various package configurations that were dipped (without any anomalous behavior possibly attributable to thermo-mechanical damage from solder dipping)

Table 4-4: Maximum and minimum values assessed for different package configurations

Package configuration	Ratio of die-area to package thickness (mm)		
	Minimum value assessed for no thermo-mechanical damage	Maximum value assessed for no thermo-mechanical damage	Value assessed for part-types that showed thermo-mechanical damage due to the environmental exposure and not due to solder-dipping
SOP	0.95	3.68	NA
SOT/SOD	0.06	0.18	NA
PQFP	2.64	9.49	10.53
PLCC	2.94	6.84	NA
TO	0.02	0.02	7.71
PDIP	0.40	1.06	NA
LCCC	0.64	0.64	NA
CERDIP	0.90	3.48	NA

4.3.4 Additional observations on the changing of die geometry over time

Tracking of parts over time may be necessary even after once successfully qualified for solder dipping.

Die shrinks (scale changes) are common in the semiconductor industry as a path to higher profits for the part manufacturer. Mask changes involve a layout alteration of the die with or without die shrink. They are often associated with process changes. Process modifications occur at fabrication on a regular basis to improve productivity and yield. Process upgrades can occur once a week; more often in newer technologies. Usually product change notices (PCN) are only issued if there is a change in the form, fit, or function of the part (affecting performance within the manufacturer's specified conditions) as defined by the manufacturer.

The change notification procedures generally used by semiconductor manufacturers are outlined in EIA/JEDEC Standard 46-B. Any change that affects the form, fit, function, or reliability of a part is considered major and requires customer notification. Any change that does not affect these factors is considered minor and does not require notification unless special contractual agreements exist. The major changes listed in the Standard are shown in the first column of

Table 4-5 below. The second column of the table contains comments on the possible impact the change on solder dipping effects. Of course, at some level all changes can impact the thermo-mechanical effect of solder dipping; the comments here are meant to cover the practical situations for decision making.

Table 4-5: Part changes and their potential impact on solder dipping

Major Change	**Potential Impact on Solder Dipping**
Manufacturing site, process flow, materials, wafer diameter, mask.	No immediate effect is expected
Assembly site, materials, marking, package style.	No immediate effect from assembly site and marking. Obviously, a package style change will impact the whole decision making process since the new package style and its geometric factors must be assessed. Material, particularly molding compound changes, can impact the

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	adhesion strengths between layers and can impact the thermo-mechanical strength. In this study, we did not control the mold compound. Before proceeding with solder dipping, one must evaluate the actions taken by the part manufacturers in assessing the adhesion strength of the new molding compound.
Test elimination.	Not of immediate concern unless the test elimination is for thermo-mechanical strength of the parts.
AC or DC data sheet parameters.	No immediate impact is anticipated. If a full TMTI type assessment is to be performed, then the electrical tests will need to use the new electrical limits for the tests.
Case outline, package tolerances.	Changes in die dimension are assumed to be included in this category of changes. The effects of die dimension changes are discussed in Section 3. The effects of the case outline change can also impact the figure of merit used in the similarity assessment.
Carrier tape dimensions, maximum storage temperature, dry pack requirements.	Changes to maximum storage temperature and dry pack requirements may potentially impact the ability of parts withstand high temperature exposure and humidity. Dry pack requirements may change when there is a change in MSL level.

The most common change notification path is through distributors since most product manufacturers purchase parts through distributors. Part manufacturers send PCNs to distributors, who then pass them on to customers who have recently purchased parts. Since the distributor personnel may not be as technically adept as the users, it is incumbent on users to assess the impact of the changes.

4.3.5 Additional observations on the part types not considered in this study

The whole TMTI study is a snapshot in time. The parts selected for the study were limited by budget constraints and focused on the needs of the study sponsors. In no way may they be considered to ‘cover’ the multitude of part types available in the commercial market place. This section listed and discussed some of part variations that were not consider in the study that could have an impact on their ability to successfully undergo solder dipping.

Parts with an attached heat spreader that are attached to the board by solder are not included in this study. If such parts are to be considered for solder dipping, the position of the die in relation to the heat spreader must be considered since there is a possibility that the die may be in close proximity to the heat spreader.

There are some new packages with exposed die pad such as QFN (quad flat no lead) and SOT638-1 packages. The impacts of solder dipping these parts are not investigated in this study.

5. TECHNOLOGY READINESS TO USE ROBOTIC SOLDER DIP ECONOMICALLY WITH CIRCUIT BOARD BUILDERS AND SUBCONTRACTORS

It is recognized that many military contractors have immediate solder-dipping needs. Although a single company performed the solder dipping for this project any vendor possessing the requisite equipment, expertise, and ability to employ the assessed robotic solder-dip process could be used. The use of vendors providing dipping processes that differ from the guidelines contained herein may prove acceptable; however, that is a choice to be made by the program requiring the services and results may differ significantly from the results seen in this research.

Early on in this research project, it was recognized that the builders of hardware for the military would most likely use robotic solder dip if it was both easy to use and ready to use - in a business sense - as soon as the project was completed. This ease of use particularly extends to subcontractors and company sites that are often used for circuit board production. Therefore, project participant Raytheon independently funded and developed a pilot 'commercialization' experiment in parallel with the TMTI ManTech Research Project. Raytheon worked with Avnet, Inc., a well-known electronic parts distributor and qualified Raytheon supplier, to develop a process by which a manufacturer (e.g., military contractor) can order some parts from Avnet that are only available with a pure tin finish from the part manufacturer and have them delivered from Avnet as tin-lead. That is, for this experiment; Avnet buys the parts, has them dipped per the TMTI process, and delivers them to the user ready for use. Raytheon's goal is that if one of their programs needs to use a TMTI solder-dipped part in a particular assembly, it simply specifies that to the subcontractor with the stipulation that it be ordered directly from Avnet. Avnet would then obtain the part, have it robotically solder dipped by a vendor with an approved TMTI process and controls. In this way, the TMTI solder dip process becomes transparent to the subcontractor, with no change in the way it is used to doing business.

The concept of placing solder dipping orders through a distributor to be more economical is based on the volume discounts associated with large orders. When a distributor aggregates orders from multiple sources, the combined volumes reduce the processing costs per part at the solder dip vendor, enabling it to offer quantity discounts that more than offset the handling costs charged by the parts house. The net result is that the ordering contractor gets the solder dipping at a lower price; the more contractors placing orders, the better the discounts. Furthermore, the contractor has eliminated his involvement with the solder dipping, which now becomes part of the purchasing procedures for electronic parts.

Numerous meeting and workshops were held at Raytheon Missile System (RMS) to develop this potential concept for "commercialization" of TMTI: Phase 1 involved establishing business relationships between Corfin Industries (the robotic solder dipper for this project), Avnet (the parts distributor for this project), as well as a review of AEM, Inc., a company that can refinish tiny chip capacitors and resistors from pure tin to tin-lead with a proprietary process. These companies have all participated in the CALCE Tin Whisker Group. Phase II involved conducting an experiment at RMS with the SM-3 missile program. This project incorporates the ordering infrastructure necessary to test the readiness for commercialization by Raytheon program managers. An immediate result from this experiment identified in Phase II was the need for a knowledgebase to determine if a part was only available in pure tin, and if so, could it

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be solder dipped? Whether or not a part could be solder dipped to replace the pure tin with tin-lead (SnPb) is being answered by this TMTI project. Determining if a part is only available in pure tin is more challenging, since the part manufacturers are making changes daily, and out of scope of this research.

However, the commercial electronics world that is driving the changes needs to know if they can get the part in lead-free. Their knowledgebase needs are therefore somewhat parallel to those of the Navy. Distributors such as Avnet are evolving databases that will eventually provide that information. Until then a joint effort by distributors and the ordering contractor is required to be sure that the part desired is only available in pure tin and that it can be solder dipped.

5.1 SELLECTED POINTS OF CONTACT FOR CONVERTING TIN-PLATED PARTS TO A TIN-LEAD SURFACE FINISH

This section lists some of the strategies that may be adopted by electronic part users who are exempt from lead-free legislation and who wish to avoid the use of pure tin parts. In addition, CALCE (or any other TMTI project participant) may be contacted for further information regarding the analysis that was carried out to qualify the parts for solder dipping and, any customized modifications to the dipping process/electronic parts that may be made by the part user.

5.1.1 Buying tin-plated parts, but having them delivered with a tin-lead finish, via the Avnet distributor

Avnet is one source that now accepts orders for the purchase and post-processing of some tin-plated parts and delivers them with a tin-lead finish. This involves the use of the replating processes for chip parts at AEM and the TMTI Robotic Solder Dip processes at Corfin Industries for microcircuits and transistors. Avnet's point of contact as of 2005 is Dave Berryhill (520-247-3510). We caution that many companies are looking at replateing parts, new companies may be getting involved daily; we have not attempted to survey the entire industry as part of this research.

5.1.2 Converting existing microcircuits and transistors from tin to tin-lead surface finish per the TMTI processes

The TMTI Project has outlined one process for the qualification of a Robotic Solder Dip Processes at Corfin Industries to replace the tin on parts with a tin-lead surface finish as described in this report. The contacts at Corfin Industries include Don Tyler and Tom Hamel (both at 603-893-9900).

5.1.3 Converting existing chip parts such as chip caps and resistors from tin to a tin-lead surface finish

AEM, Inc. reports that as of mid-2005 it has processed over 85 types of orders to replace the tin plate on chip capacitors and resistors with tin-lead plate. The processes used are AEM's proprietary processes. AEM contacts Jeff Montgomery and Gary Miscikowski can be reached at 858-481-0210, ext. 1333 and 1322 respectively.

5.1.4 Intercompany relationships experiment for a potential "TMTI commercialization" effort

This phase of the research and experimentation was primarily facilitated by Bill Rollins at RMS who is available for consultation by anyone interested in pursuing a similar path with the same or other suppliers. Mr. Rollins can be reached 520-794-5203.

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6. PROCESS DEFINITION FOR THE ROBOTIC SOLDER DIP

All solder dipping for the TMTI project was done at Corfin Industries in Salem, New Hampshire. Corfin was an original member of the proposal team for the Project. Any company possessing the requisite equipment and expertise would be a candidate to provide robotic solder- dip services employing, as one method, the process qualified by this TMTI project. When the project was begun, the requirement for Corfin to disclose the processes that were used in the solder dip for this test was mandated so that the TMTI robotic solder dip processes could be placed in the public domain. Corfin was not required to disclose how they maintained their process, only what was achieved. Therefore, other companies that can maintain the precision required by those processes should be able to replicate the same successes that were achieved in this project.

6.1 SOLDER DIPPING PROCESS

Standard solder-dip processes broadly consist of the following five stages shown in Figure 6-1: fluxing, preheating, dipping, water rinsing, and drying. Fluxing aids in improving wetability through removal of oxide films, while preheating activates and dehydrates the flux and reduces the thermal shock experienced during dipping. Dipping dissolves the original finish and replaces it with a eutectic tin-lead finish. Rinsing cleanses any residues on the part that may accumulate during prior steps. The part is then dried to remove excess rinsing agent.

In the TMTI study, solder dipping was used as a post-manufacturing retrofit method to “refinish” parts by means of replacing the preexisting tin finish with eutectic tin-lead. The parts were baked for 24 hours at 150 °C and maintained in accordance with MSL 5 of J-STD-033B prior to processing. This bakeout level ensured that any possible human errors in recording and reporting the part moisture exposure levels would not cause any problems during dipping. Parts were presented to the robotic handler on trays. The robotic arm was configured for either vacuum pickup or mechanical clamping using titanium fingers. Only the device body was contacted to ensure leads were not deformed and original co-planarity was maintained throughout the process. The full lengths of the leads on each side were fluxed using Superior No. 30 organic acid, water-soluble flux for 1.0 ±0.1 second. Excess flux was then blown off. The part was then moved into the forced hot-air preheater at 150 ±3°C for a 4.0 ±0.1 second dwell. At the solder wave, the full length of the leads on each side was immersed in Sn63Pb37 solder at 245 ±1°C for 3.0 ±0.1 seconds per side. The robotic motion was customized for each package type to allow for even solder thickness without bridging of solder between leads. Solder thickness varied based upon the size of the surface area and co-planarity was maintained within 0.004 inch. Following the solder, flux residue was removed by back-and-forth motion in the 60 ±3 °C ultra-filtered water at the wash station. The wash solution was emptied and refilled with fresh liquid between each part’s wash cycle to prevent an accumulation of contaminants. Parts were passed through forced air for drying and then returned to the pickup location.

The process made use of mechanized robotic handling of parts with features of constant specific gravity control while fluxing and nitrogen blanketing during dipping. The full length of leads up to the package edge was immersed in the hot solder bath during dipping. Robotic motion programming was customized according to part type in terms of angle of emersion and rate of withdrawal (during dipping). This allowed for minimizing contact surface and helped to produce

a thinner finish coating designed to ensure no bridging between leads, especially for high-pin count fine pitch parts.

The solder dip processes used in the TMTI study were identical to traditional standard processes, with notable exceptions of solder temperature and pre-process baking of the parts. Standard processes use the same alloy at 260°C and do not require baking prior to processing. Moreover, flux material and accumulated dwell periods used in standard processes may be varied depending on the original, preexisting finish in standard solder-dip methods. In this project, however, these factors were maintained as invariants, regardless of the original finish material, solder dipping to ensure uniformity in the analytical comparison of results. T here was also no acid precleaning prior to processing.

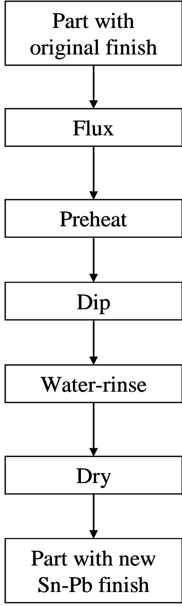

Figure 6-1: Solder dipping process flow

6.2 ROBOTIC SOLDER-DIP EQUIPMENT USED

Two models of equipment were used based upon availability in the production schedule, but each model is capable of performing all the processes. Both models, LRT-2020 and LRT-3000, are manufactured by Corfin Automation LLC and feature robotic handling with either a vacuum or a mechanical pickup mechanism, a 275-lb-capacity dynamic wave solder pot with nitrogen blanketing at the solder surface, forced air preheater, and a 3-gallon flux pot with dynamic wave and constant specific gravity control. Electrostatic charge was maintained below 50 volts throughout the process. Using this equipment, robotic hot solder-coating replacement processes were developed for each package shape and size to provide a high quality tin-lead immersion finish on the parts.

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7. RISKS ASSOCIATED WITH SOLDER DIPPING

There is a long history available for the use of solder dipping for hermetic and insertion-mount parts; however, this is not the case with surface-mount devices because their fine pitch and high-density characteristics made solder dipping difficult and risky. Now that robotic dipping offers promise for use in programs wishing to use surface mount technology while maintaining high reliability, an investigation of the effects of this process and a study of associated risks assumes increased importance.

Concerns with solder-dipped finishes include non-uniformity in finish thickness with potential for base-metal exposure, increased growth of intermetallics due to high temperature exposure, dissolution of the original finish, thermo-mechanical damage within the package due to the thermal shock experienced during dipping, solderability of the refinished terminations during printed circuit board (PCB) assembly, and potential in change in MSL value due to dipping.

7.1 QUALITY OF THE SOLDER-DIPPED FINISH

If the solder-dipped finish thickness is not uniform all around the termination cross section, gaps may occur exposing the base metal that adversely affect solderability. The non-uniformity in thickness can arise due to surface tension effects of the molten solder and the geometry (curvature) of the termination cross section. In the worst case, base metal of the lead frame may be exposed at the corners. The risk of base-metal exposure may be pronounced for high-pin count parts where the lead frame is usually manufactured by means of etching as opposed to stamping. The curvature of the termination cross section in etched lead frames is usually concave, while that of stamped lead frames is convex. A related potential issue with the process under review is whether the process dissolves the preexisting finish and replaces it with the new solder-dipped eutectic tin-lead finish. The first test run as part of TMTI was to cross section some dipped parts and verify with SEM-EDS that this has occurred.

Another finish-related quality issue concerns intermetallic compounds (IMC) that are formed due to solid-state reactions between the finish material and base metal of the lead frame. IMC growth is dependent on temperature and time. These are brittle, have poor wettability characteristics, and can affect solderability performance. The concern with the solder dipping process was the potential for increased thickness of intermetallic growth due to the high temperature experienced during dipping. Moreover, if the finish itself is not sufficiently thick, formation and growth of the intermetallic, which is continual in nature, may either consume tin from the finish material and eventually expose the base-metal of the lead frame or result in formation of a readily oxidizable, lead-rich zone. Either condition could adversely affect part solderability.

7.2 DELAMINATION AND THERMAL DEGRADATION OF THE PACKAGE

Exposure to the thermal shock during dipping makes delamination and subsequent package cracking a potential reliability concern. Moisture absorbed by the organic materials (mold compound and die attach) in PEMs during shipping and storage may evaporate at the high temperatures experienced during dip. The steam pressure thus generated makes poorly adherent internal surfaces vulnerable to delamination. This may make the part more susceptible to

popcorning during PCB assembly reflow. Also, if coefficient of thermal expansion (CTE) mismatches between silicon, the mold compound, the die attach and the leadframe material exist, the thermal shock experienced during solder dipping and subsequent cool down may induce residual thermo-mechanical stresses in the part. In the worst case, stress related failures such as cracked passivation and metallization deformation might result. A number of studies on silicon chips in molded plastic packages indicate that the probability of such thermo-mechanical damage is higher at the die edges than towards the center of the die. For TMTI, acoustic microscopy was used at all stages of the testing to monitor for any delamination that may have occurred.

7.3 ROBOTIC SOLDER DIPPING MAY DETERIORATE A PART'S MOISTURE SENSITIVITY LEVEL (MSL)

This is a possibility that was not tested due to the need to solder dip as many package styles as possible on the limited funding available. To be conservative, the use of the allowable exposure schedule of parts that is one MSL level worse than the original parts is recommended.

8. TEST DEFINITION AND DESIGN

This section discusses various issues that were considered for the design of the qualification tests for the solder dipping process and selection of parts to be solder dipped. It further presents overall process flows of the test plans that were chosen and some results from the electrical functional tests performed on the parts.

8.1 TEST PHILOSOPHY CONSIDERATIONS

For tests to succeed, the epoxy used as an encapsulant for the parts to be solder dipped had to bond well to the lead frame fingers as well as the die. There are hundreds of epoxy formulations on the market that vary by manufacturer, and the specific one used on any given part is not included in the normal data book information. The saving grace from the obvious dilemma of how to ensure the tests were applicable to a broad array of part types without having to test literally thousands of combinations of packaging styles and encapsulants is the well-established trend in new epoxies to be better than their predecessors. The actual parts used in this test were built in spring 2004 or earlier, with some vintage 2001. Users of this report will, for the most part, be using newer tin-plated parts intended for use with the higher reflow temperatures required for lead-free solders. The parts will have the more recent improvements in the epoxy encapsulant to accommodate those higher temperatures and should perform as well as (or better than) the actual parts used in the TMTI tests.

Another factor related to encapsulant strength is the stress applied to the bond. The stress of interest is that associated with the solder dip temperature profile as it relates to the comparative thermal conductivity between the lead frame material and the encapsulant material; equally important is the mass or volume of those materials used in a particular packaging style. The CTEs for the lead frame material and encapsulant are usually matched in the package design which is why alloy 194 (mostly copper) is most often used with epoxy packages and alloy 42 (iron nickel) is most often used with ceramic packages. However, the thermal conductivity of the lead frame alloy is about an order of magnitude greater than the encapsulant, so the amount of lead-frame material being solder dipped on any package style will be the dominant factor in determining the temperature gradients inside the package. The time-related dynamics of those temperature gradients will determine the amount of stress applied to any potential failure site. Again, the key issue here is the volume of the termination materials (such as copper-based leads) and the encapsulant used in each package, which also accounts for the need to test each package style. Section 4 provides a more detailed discussion on “Qualification by Similarity” that addresses the thermal-mechanical robustness of a package as a function of the ratio of die area versus the package thickness.

A statistically valid sample of each packaging style was used in the test.

8.2 PROGRAM FACTORS DETERMINING TEST PACKAGE STYLE SELECTION

Since this Navy project was conducted on a limited budget for time and money, there were a number of filters applied when selecting the part package styles to be included in the test. First, the test goal was to select package styles in current and near future use that were applicable to Navy programs, with a bias toward the STANDARD Missile (SM-2 and SM-3) programs that sponsored the project. Within the confines of the $1 million budget and 1-year timeframe, we

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chose a mix of ceramic and plastic encapsulated package styles representing a mix of manufacturers, lead frame materials, MSL, cost, availability, testability (and its related cost and schedule), and market life. With all part packages chosen needing a good probability of passing the planned test, their selection was based on the CALCE Consortium's experience from many years of part failure mode investigations. The parts also had to have a lead configuration that the dipping organization could successfully solder dip without bridging the solder across lead spacing. The team, Navy BMPCOE, Raytheon's Tucson and Tewksbury sites CALCE, and Corfin's part selection team spent several months in trade-off studies, with concurrent inputs from the CALCE Tin Whisker Group.

8.3 TEST DESIGN & EVALUATION

Twenty-three different electronic part types were evaluated to assess the effects, if any, on their electrical functionality and long-term reliability produced by robotically solder dipping the entire length of their leads. Testing and evaluation of these parts was performed by Raytheon's Reliability Analysis Laboratory facilities in Tewksbury and Andover, Massachusetts. A detailed test report was written covering the results of testing of each of the part types. This report provides a summary of the results of those tests and evaluations. Destructive physical analysis (DPA) was also conducted on selected parts at the CALCE failure analysis laboratory. Overall results are included herein; however, detailed write-ups are contained in separate CALCE documents.

The 23 different electronic part types under evaluation are summarized in Table 8-1 below. These parts have been sorted into three different groups for the purposes of evaluation. The first group includes all of the hermetic, ceramic packaged devices. The second group consisted of PEMs on which no MSL evaluations were (or are) planned. Although MSL testing was a part of the project, parts have been identified and set aside so that such evaluation can be performed in the future. These parts comprise the third group.

Each group of parts was subjected to a unique, though similar, test and evaluation flow. Flowcharts describing each of the three basic flows are shown in Figure 8-1, Figure 8-2 and Figure 8-3. A color-coding key is provided in Figure 8-4. Environmental test conditions were as follows: temperature cycle test [-55°C to 125°C] for 150 cycles with 10 minute dwells followed by temperature-humidity test at 85°C/ 85% R.H. for 500 hours/ 21 days.

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Table 8-1: A listing of the 23 part types, identifying the test flow applied to each and the referenced electrical test report number

Part Number	Package Type	Functionality	Manufacturer	Report number	Test Flow	Electrical anomalies from solder dip
MMBT2222ALT1	SOT 23	Bipolar transistor	ON Semi	a2004-01486-R1	MSL Plastic	None
IDT720415SOI	SOIC-28	CMOS ASYNCHRONOUS FIFO	INTEGRATED DEV. TECH. INC	a2004-01604-R1	MSL Plastic	None
ADG608TRU	TSSOP 16	Analog	Analog Devices	a2004-01837-R1	MSL Plastic	None
IDT72V11081	PLASTIC, TQFP-32	3.3 VOLT CMOS SYNCFIFO	INTEGRATED DEV. TECH. INC	a2004-01838-R1	MSL Plastic	None
EPM256SRC208-7	208 pinpower quad flat pack	Eraseable PLD	Altera	a2004-02389-R1	MSL Plastic	None
EPM7128TI100-10	100 pin plastic thin plastic quad pack	Eraseable PLD	Altera	a2004-02392-R1	MSL Plastic	Possible[1]
DAC8412FPC	PLASTIC, LCC-28	QUAD DAC	ADC	a2004-02395-R1	MSL Plastic	None
IDT7201LA12J	PLASTIC, LCC-32	AsyncFIFO, 5.0V	IDT	a2004-02397-R1	MSL Plastic	None
54ACT00LMQB	54ACT00LMQ B	CERAMIC, LCC-20	QUAD 2-INPUT NAND GATE	a2004-01487-R1	Hermetic	None
DS26LS32MJ	16 lead ceramic dip	Quad diff. line rec.	NSC	a2004-02391-R1	Hermetic	None
LT1058MJ/883B	CERDIP-14	QUAD OP AMP	Linear Tech.	a2004-02394-R1	Hermetic	Possible[2]
AM26LS31DC	CERAMIC, DIP-16	Quad Differential Line Driver	TI	a2004-02396-R1	Hermetic	None
SN75ALS195J	16 lead ceramic dip	quad differential line receiver	TI	a2004-02398-R1	Hermetic	None
OP490AY	CERDIP-14	QUAD OP AMP	ADC	a2004-02399-R1	Hermetic	None
OP284ES	8-lead SOIC	Amplifier, Operational	Analog Devices	a2004-01481-R1	NON-MSL Plastic	None
1N4148W-7	SOD-123	Diodes and discrete	Diodes Inc.	a2004-01482-R1	NON-MSL Plastic	None
74HC00N	PDIP 14	Logic	Fairchild	a2004-01483-R1	NON-MSL Plastic	None
74HC540N	PDIP 20	Logic	Fairchild	a2004-01484-R1	NON-MSL Plastic	None
74AC14SC	SOP	Logic	Fairchild	a2004-01485-R1	NON-MSL Plastic	None
2N3906	TO-92	Small signal transistor	On Semi	a2004-01605-R1	NON-MSL Plastic	Possible[2]
EPM7256AQC208	208 pin plastic quad flat pack	eraseable PLD	Altera	a2004-02393-R1 a2005-01434-R1	NON-MSL Plastic	None
SI4967DY	SO	Transistor	Siliconix	a2004-02805-R1	NON-MSL Plastic	None
FQFP47P06	TO-220 (3-lead)	MosFET	Fairchild	a2004-03411-R1 a2005-01431-R1	NON-MSL Plastic	None

Notes: 1. Not qualified 2. Subsequent analysis at CALCE determined that dipping did not damage part.

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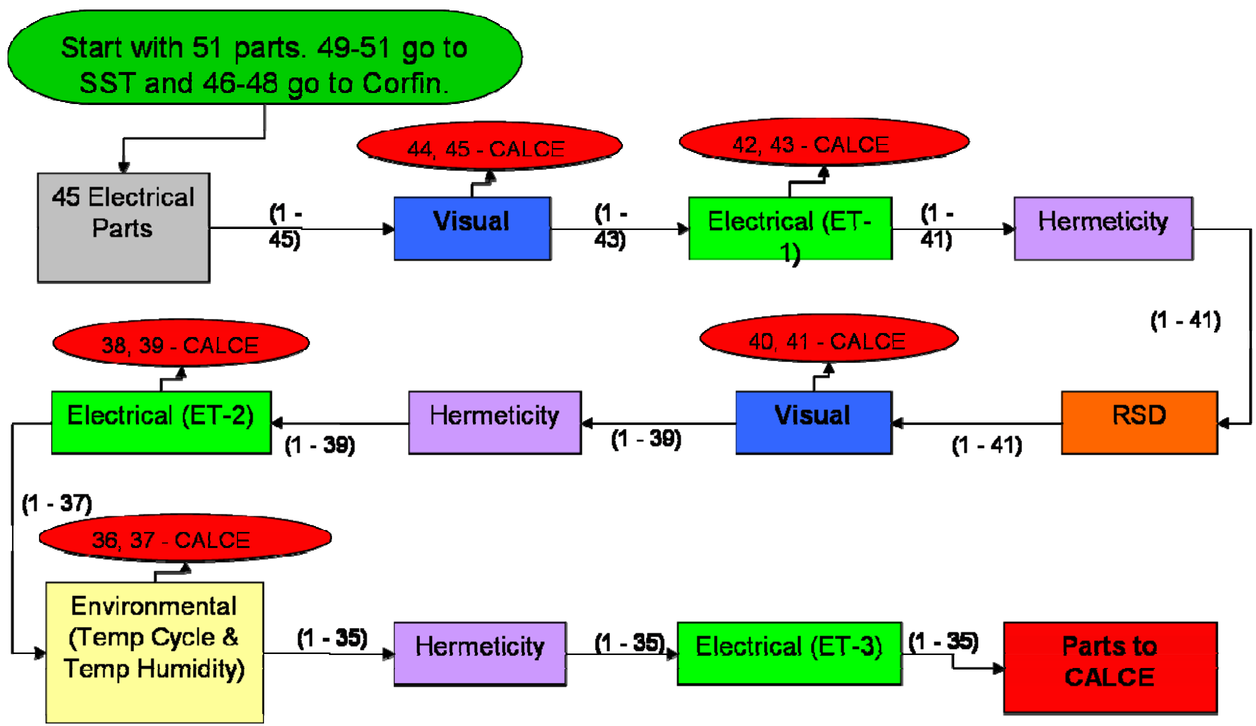

Figure 8-1 : Test flow for hermetic parts

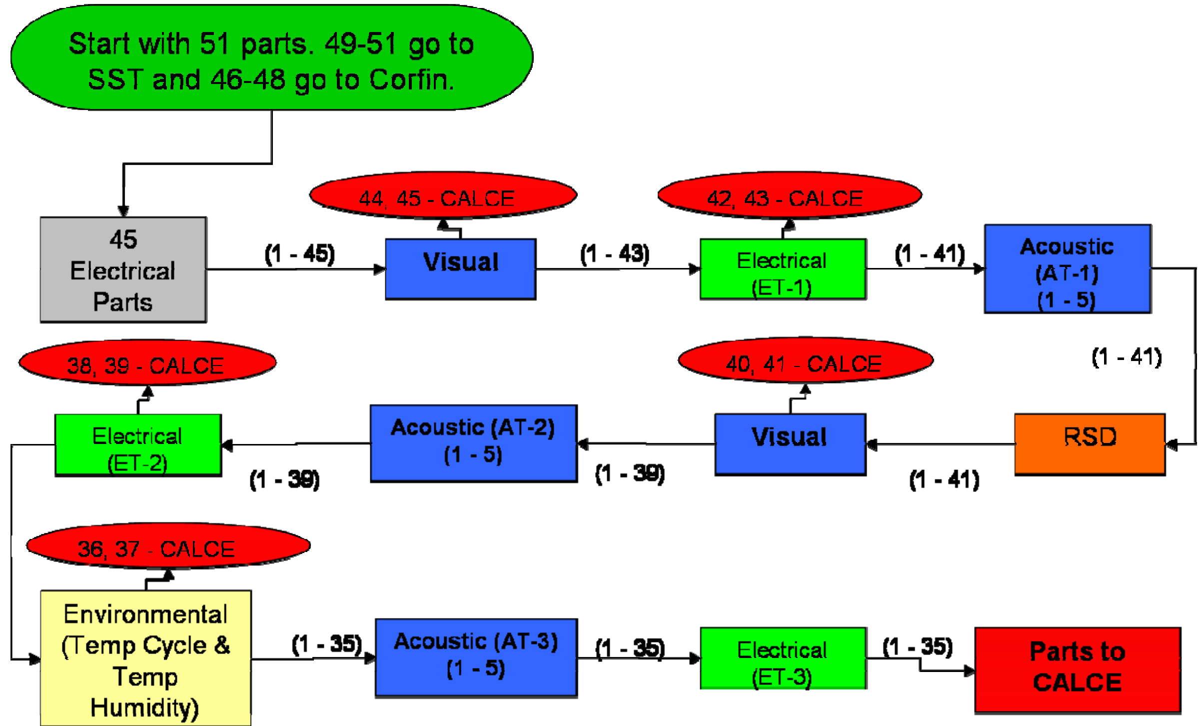

Figure 8-2 : Test flow for non-MSL PEMs

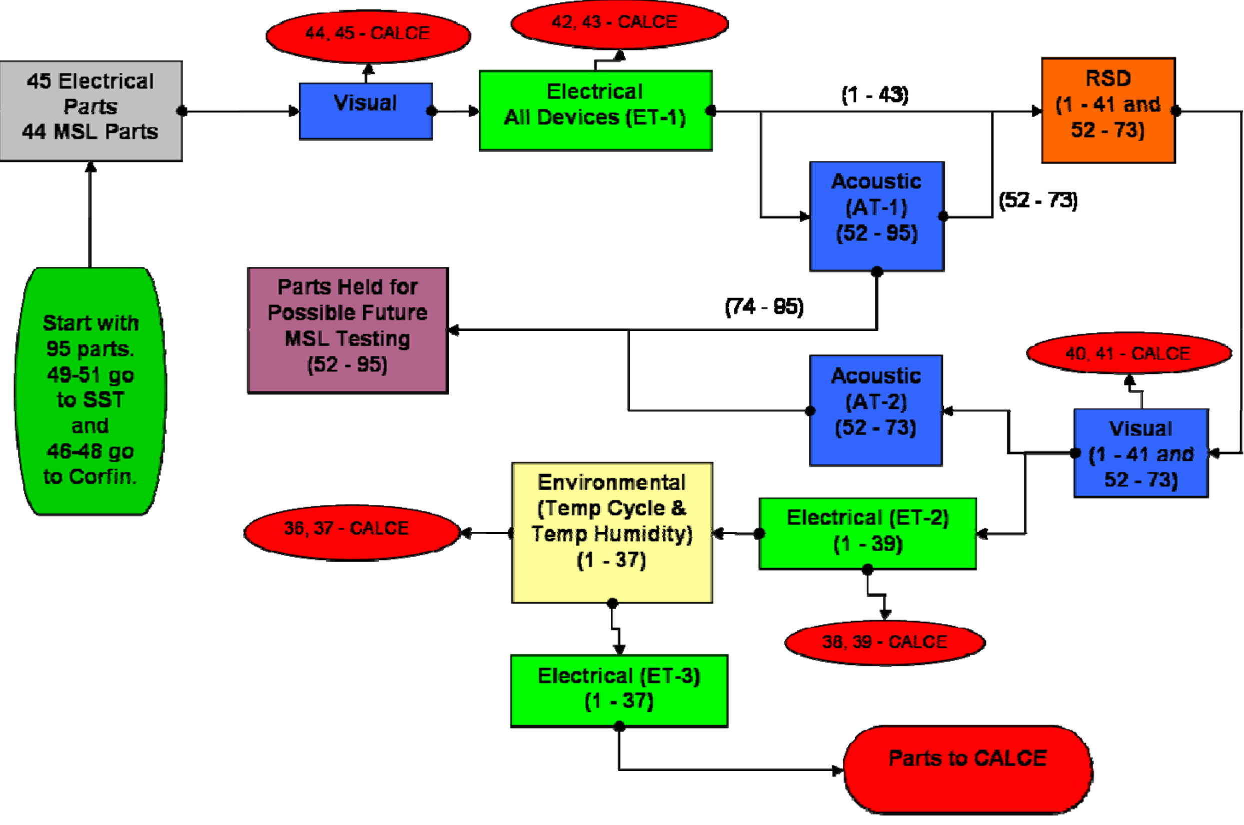

Figure 8-3 : Test flow for MSL PEMs

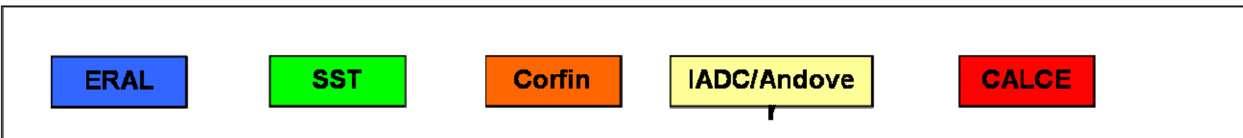

Figure 8-4 : Color coding key

Evaluations were performed at the Reliability Analysis Laboratory in Tewksbury Massachusetts. Most of the electrical testing was performed at, SST, Inc., a subcontracted testing laboratory located in nearby Burlington, Massachusetts. Some of the electrical testing and all the environmental testing were performed at the Environmental Test Laboratory at the Raytheon Integrated Air Defense Center in Andover, Massachusetts. Prior to the evaluations and at various times during the evaluations, selected parts were shipped to the CALCE laboratory at the University of Maryland. Following all functional and environmental testing, all parts were shipped to CALCE. Additional evaluations, primarily DPA, were performed by CALCE as previously stated. Those results are reported in separate documents.

8.4 ELECTRICAL TEST RESULTS

None of the 23 parts (part types) evaluated displayed evidence of damage or degradation directly attributable to the robotic solder dip process itself. One device type, part number (PN) LT1058MJ/883B, a hermetically packaged Quad Differential Line Receiver, was noted to experience minor shifts in its electrical performance at extremely cold temperature after environmental tests. These shifts were within the specified limits for these devices. Further analysis must be performed to determine whether these shifts are in any way attributable to exposure of these parts to the robotic solder dip process.

Another device type, a Digital IC, PNSI4967DY, Dual P-Channel MOSFET, in an SO-8 package, suffered numerous test-related failures. Twenty-one devices failed catastrophically the first time they were tested (prior to the planned solder dipping step). Several actions were taken at the test facility to improve the testing. Replacement parts were obtained, and this testing was repeated. Four additional parts failed catastrophically during electrical testing later in the test sequence. Each of these failures was determined to have been induced by the testing. These parts have particularly small leads through which significant amounts of current must pass. This creates a situation where small amounts of contact resistance between the lead and the test set can result in a condition where catastrophic failure occurs. A total of 31 devices made it through all three electrical tests. The results on these parts indicate that robotic solder dip introduced no deleterious effects.

Most of the Digital IC MOSFET, TO-220F devices (PN FQFP47P06) displayed significant increase in gate-to-channel-leakage current during high temperature testing following environmental exposure. Later retest showed a decrease in leakage, although not to the original measured levels. These results imply that moisture (and possible contaminant) ingress occurred during the environmental portion. Additional testing was performed to determine whether these leakages after environmental testing were in any way related to the robotic solder dip process or if they reflected an innate condition of the parts. The entire test sequence was repeated on an identical population of parts, but this time the robotic solder dip step was omitted. The electrical results after environmental testing were quite similar to the results obtained on the solder-dipped

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group. This indicates that the robotic solder dip process was neither responsible for the leakage condition nor did it exacerbate this preexisting condition.

One of the very small parts (SOD–123, 1N4148W-7) that was evaluated was observed to develop significant accumulation of solder relative to the very small dimensions of the leads. The presence of solder balls was detected during visual examination on several of these parts. This condition resulted in some difficulty in obtaining electrical test data due to problems with making good contact to the terminations. No electrical anomalies were induced as a result of the robotic solder dip process. However, this experience indicates that special care may be required in applying solder dip to parts that utilize very small termination areas.

Unfortunately, the complex test flow required for this study necessitated the numerous handling of parts, resulting in mechanical damage to the leads of some of the parts. Test parts were also packaged for shipping and handling to specifically accommodate the small number of devices involved. During normal production operations, packaging of the parts should provide protection superior to that provided the parts in this study. The amount of handling involved with production parts will also be substantially less, greatly reducing the opportunity for mechanical damage. Therefore, the mechanical damage observed on some of these parts is not considered representative of what would be expected with production hardware subjected to robotic solder dip

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9. TEST RESULTS THAT WERE USED TO CREATE THE REPORT

For each part, the analysis was performed on a total of 45 samples: 2from each of the following 5 stages and 35 at the end of the "after-environmental" stage:

1. As received
2. After electrical stage 1 testing
3. Post-dip
4. After electrical stage 2 testing
5. After environmental testing

Refer to report number CALCE/IdentificationCodes/25 for a summary of identification codes used for the 45 samples under study. Refer to Figure 9-1for the schematic of general test flow. Two samples were set aside at each of the five stages mentioned above as control samples for failure analysis that focused on reliability failure modes. Each control group set aside (the two samples from every process stage) was exposed to the same tests. A comparison of test results of these sample sets at different process stages provided a means for assessing the effects of the solder dip process on the part. The flow described below is for plastic package parts. For ceramic parts, the process was appropriately modified.

One part from each control sample set was subjected to Scanning Acoustic Microscopy (SAM) to detect delamination, if any, at critical interfaces including the dietop and molding compound, die paddle top and lead fingers-molding compound. A combination of C-scans and A-scans utilizing pulse-echo transmission techniques with both peak-amplitude and phase inversion modes (as applicable) was used to detect delamination, if any, at these interfaces. Figure 9-2 is a sample of a C-scan, A-scan output.

The working principle of SAM is that for any change in acoustic impedance (such as at an interface between two materials), a portion of the ultrasonic signal is reflected back, while the remainder is transmitted through the interface. Two modes of inspection are used: 1) pulse echo mode, in which the ultrasonic signal reflected back to the transducer is used to produce a digitized image and 2) transmission mode, in which a second receiving transducer examines the ultrasound transmitted through the sample to produce an image.

The A-scan is the actual waveform of the acoustic signal obtained, while the C-scan is the digitized image produced by raster scanning over the entire surface area of the sample under examination at a given depth as determined by the placement of the "datagate." The data-gate is the interface of interest within the thickness of the sample determined by positioning a rectangular frame on the A-scan. The larger the time value associated with the dataate on the time axis of the A-scan, the greater the depth of the interface of interest. Thus, by moving the gate position in time on the A-scan, one can image different depths within the sample. A C-scan in other words, records the peak amplitudes from a certain depth (determined by the data-gate placement) within the sample. Based on the strength of the reflected signal, each pixel is mapped to a gray scale color. A pixel with high signal strength is assigned a lighter shade of gray compared to one with lower signal strength. If air is present at an interface, the entire ultrasonic signal from that particular region is reflected back, translating into bright areas on the C-scan. The presence of air pockets in terms of delaminated regions or voids would also cause the shape of the A-scan waveforms (taken at different points over the interface of interest) to be different in the data-gate region, not allowing them to overlap. Severe delaminations will cause phase

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inversion of the A-scan signals at the data-gate region. Phase inversions may be further detected by means of enabling the phase gate over the data-gate region. Phase-inverted regions will appear in different colors over the digitized C-scan image only when the phase gate is enabled.

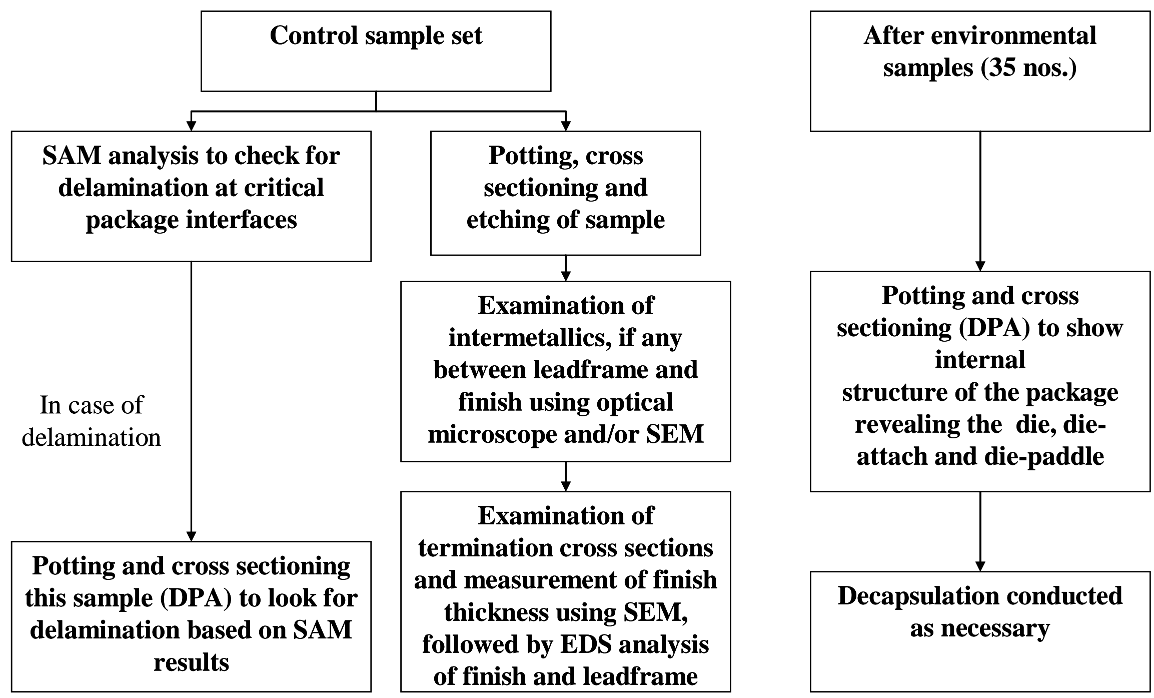

Figure 9-1 : Overall test flow

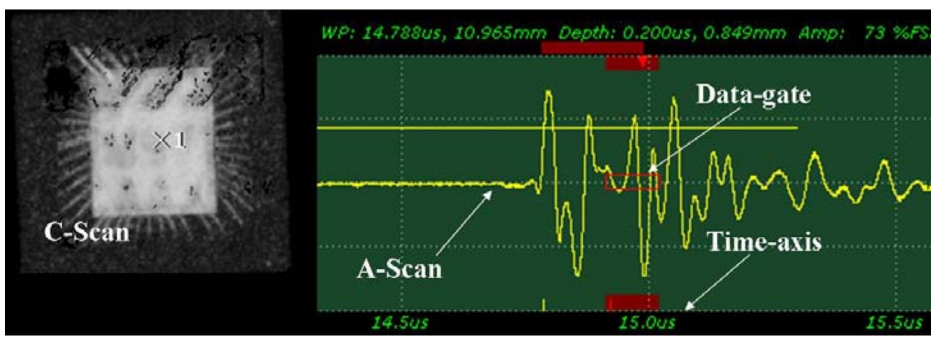

Figure 9-2 : Figure showing sample C-Scan and A-Scan

In addition to the control sample sets of parts received at the CALCE laboratory at each of the five process stages as described above, a lot of 35 "after environmental" samples was also received. Three of these samples underwent Destructive Physical Analysis (DPA), where a planar cross section through the center of the package was taken, revealing the die, die-attach, die paddle, lead fingers, and the molding compound. A standard solution of 10 parts of resin and 3 parts (by weight) of cross linker (hardener) was used for potting and sample preparation. Curing time was in excess of 6 hours. Cross sectioning was done through a combination of rough

grinding using 60-, 240-, and 400-micron sand papers; fine grinding using 600-, 800-, and 1200-micron sand papers, and finally fine polishing using alumina powder. The cross sectioned package was then examined using the optical microscope for the presence of any gross delaminations.

When a part was found to have a unique combination of plating and lead-frame materials; this was identified as one of the parts earmarked for intermetallic study to be conducted at a later date. If any significant information is derived from the intermetallic analysis, an additional report will be issued. However, it must be noted that no moisture sensitivity evaluations or solderability tests were performed for any of the parts in this project. Laboratory testing and analysis at CALCE concluded that: rigorous incoming quality control is mandatory for all parts that will undergo solder dipping; solder dipping may cause latent damage to parts and could cause magnification of any pre-existing manufacturing defects. It is therefore essential to ensure that one starts with good parts before exposing them to solder dipping.

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10. CURRENT IMPACT OF LEAD FREE ON HIGH RELIABILITY SYSTEMS

The transition to lead-free solders and finishes is adversely impacting virtually all high reliability systems. The degree to which these systems are affected depends on many factors, some of which include difficulty establishing life cycle reliability and supportability requirements for systems currently in design or nearing production, selecting suppliers and parts, and planning manufacturing processes for soldering and conformal coating. Those in production may face the need for immediate line stoppage and rework, parts non-availability, mixed technology part-tracking, supplier conformance monitoring, the need for planning early redesign, potential liability issues and others. Fielded systems must deal with supportability, reparability, and upgrade planning.

Every high reliability program should have already begun an assessment of lead-free impact. Depending on the nature of the program and its life cycle status, some or all of the following impact factors should be addressed:

- System Tin Whisker Risk Mitigation Level (reliability requirements drive the level of the tin whisker risk mitigation effort required)
- Current exposure – assess Bill of Materials (BOM) for existing tin-plated parts
- Risk assessment – relative levels of tin whisker risk incurred by system design and material selection; use of risk algorithm.
- Need for incoming inspection (e.g., X-ray fluorescence (XRF))
- Need for building surveillance hardware to continuously monitor whisker growth
- Supplier lead-free status and roadmap
- Need for employing mitigation techniques (e.g., underplating, robotic solder dip, replating, conformal coating)

The most significant impact of lead-free falls on systems where virtually no pure tin plating is tolerable. An example of this is a system characterized by factors such as: little or no redundant hardware parts/circuitry, not composed of line-replaceable units, not designed for built-in test to the circuit card level, may require long periods in dormant storage and may require extreme levels of safety.

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11. FUTURE ISSUES AFFECTING THE APPLICATION OF TIN WHISKER MITIGATION SOLUTIONS

A "Graybeard Team" was assembled to conceptualize the deliverable report, with particular emphasis on future industry issues that are unknown at this point. The "Graybeards" recruited for this team consisted of:

- Jerry Servais - retired parts manager from Delco and widely regarded expert on plastic-encapsulated microcircuits
- Bob Stanbery - retired reliability manager from Hughes Missile Systems, who is skilled at seamlessly integrating current knowledge into likely future scenarios
- Pete Temple - retired Raytheon advanced packaging expert who is widely regarded for his ability to "think out of the box"

Five teleconferences were conducted under the guidance of Bill Rollins of Raytheon. Participant comments were collected in meeting notes from which the following paragraphs were developed.

The Team decided on five specific elements to be considered:

11.1 WHAT IS THE PROBLEM?

Long-time military-mandated, non-pure tin-based solder surface finishes on electronic parts are going away because of environmental efforts, etc. Industry is approaching a milestone in July 2006 for many electronic part vendors to change to lead-free products. Many are choosing to use pure tin plate as a finish coat on part leads, and history has shown that to be incompatible with the service life needs of military electronics. The tin plate grows tin whiskers over time and can cause short circuits.

11.2 HOW DOES IT AFFECT US? (WHY DO WE CARE?)

We need to communicate the current and future challenges in a conceptual manner. The supply of basic building blocks for electronics is severely compromised. The impact of the problem on high reliability programs should be the prime focus. The primary technological solutions to the disappearing supply chain (which now will supply only tin-plated parts) are: solder dip for active parts, replating for passive parts, and the possibility of conformal coating for use when the first two don't work. However, development and qualification of these solutions are more an issue of cost, resources, and timing than is the underlying technology. Obtaining additional government customer support for this is mandatory. Because we do not have a complete set of solutions, continuing to build high reliability hardware is incurring risk that did not exist a few years ago before the supply chain tin problems started. At the present time, we have no high reliability production options where we are not already in trouble. Mission assurance and contract performance/cost issues are already at risk.

This tin crisis is a far bigger problem for high reliability products than PEMs (Plastic Encapsulated Microcircuits) ever were. We have no choice but to be successful in getting a conformal coating project funded.

The tin problem will impact all the players in the electronic assembly process. It will be necessary to educate and communicate the problem and solutions (when they exist) to those

involved, including parts vendors (commercial, niche, military), contract manufacturers, offset participants, military depots, subassembly providers, system manufacturers, and customers. Offset participants exhibit a wide range of behavior; some are helpful and want to follow the contractor's lead and some go their own way. Constant vigilance is required for many vendors. An example of a contract manufacturer would be Tyco or one of the other board assemblers. Subassembly providers are the "black box" suppliers, e.g. altimeters, etc.

The opportunity to fail increases as the number of circuits in the system increases. Since tin whisker growth is probabilistic, the opportunity for tin-caused failures will increase with the number of instances of pure tin in any system in which it is used.

11.3 WHAT HAS BEEN/IS BEING DONE SO FAR?

Creation of the CALCE Tin Whisker Group (TWG) with over 85 sites involved allowed the assessments of vendor changeover/understanding of part types involved, vendor timelines, the TMTI project, and preliminary conformal coating studies, etc. The level of TWG money and the effort commitment reflects the military/space perception of the severity of the problem.

11.4 CHANGES OVER TIME THAT COULD AFFECT THE CURRENT PROBLEMS

Likely future events that would effect the current problems (mostly from part supply sources) could include emerging technologies, government directives based on MDA's response to the war on terrorism, geo-political issues that could affect trade with the proponents of lead-free (SE Asia, and Europe), production companies outsourcing to offshore sites the engineering control functions responsible for product reliability and quality, future lawsuits from tin whisker-caused failures in commercial applications, etc.

The reality of the need for such speculation was solidified by Jerry Servais's story of what happened in spring 2004 at Delphi Automotive where some mechanical and electrical part engineering functions were split and moved to separate off-shore locations (i.e., Mexico and China).

11.5 WHAT NEEDS TO BE DONE IN ADDITION TO THE ACTIVITIES OF THE TMTI PROJECT AND THE CALCE TIN WHISKER GROUP? AND WHAT ARE THE PROJECTED FUTURE TRENDS?

a) There is no doubt that China will become a dominant player in the future parts market. Perhaps the question for the TMTI users will be whether or not that would happen in the next 4 years, which is probably the timeframe of immediate concern. After that, emerging technologies and niche industries could be more dominant in the aerospace supply market.

b) Possible driving influences for changing way from tin to other elements are lawsuits resulting from tin whisker failures during operation. Historical examples of failures of some heart pacemakers from tin whiskers in the 1970's as well as existing case law will certainly support the plaintiff's position. The tin whisker lawsuits of the future should be very lucrative for all but the defendants.

c) Communications requirements to all suppliers will be necessary if the results of the TMTI effort and other tin whisker risk mitigation efforts are to be successful in solving the Navy's tin whisker threat. Best Manufacturing Practice issues, reduction of risk mitigation cost impacts, and subcontractor flow-down problems exaggerate this challenge. The solutions coming from

TMTI and the CALCE Tin Whisker Group projects are tools that must be endorsed by the government program managers and the contractor program managers so they get used.

d) Between the custom part procurement and the conformal coating options mentioned in the Graybeard telecons, conformal coating appears to be the most useful effort. This study would probably incorporate up to eight materials and take about two years to complete.

e) The team's thoughts on evolution of the packaging as it relates to the tin problem are:

We will see continued integration, particularly at the silicon level (i.e., more functions collapsing into the single-chip package). Also, the "time–to-market" and the "life-of-product" for commercial products are unique to the commercial world, which implies rapid change relative to the military market.

Package lead-spacing will continue to shrink, which may make the commercial sector more vulnerable to tin whisker risk as well (even if their product service life may be only 3-5 years).

In some areas of product design there will be a trend toward area-array packages. Pure tin is not used in their interconnects, but they can be vulnerable to whiskers that break off from other sources. These include the computing portions of the circuitry (processors, interface chips, stacked memory) and some sensor parts (digital optical arrays and microwave diodes, for example). Smaller volume products will also eventually see "Z-stacked" custom circuits in the computing areas. Several portions will remain vulnerable such as power circuits, actuators, and bus connectors, as these will tend to use part packages with leads as opposed to the bumps used by area array packages.

f) The team does not think that "backward deployment" or retrofitting is a simple solution. United Airlines had a mandate to retrofit everything over a 20-year period, which resulted in major integration problems. Interfacing manufacturing sources is always very complicated. There are at least two impediments to retrofitting—maintaining the interface to the next assembly and timing problems (along with voltage matches) resulting from the new parts being faster than the old. There is also a question about the overall system risk assessment. It may be that reliability goes down if uncorrected tin problems are inserted.

g) There is the possibility of escalating failures due to tin, driving some commercial markets to mandate change. A possible arena is the medical market (pacemakers, instrumentation, etc.) that would likely be stimulated by lawsuits.

h) A possibility exists that there will eventually be a conversion to a plating system that does not have a whisker problem, possibly a palladium plating process similar to Texas Instrument's. This conversion would be driven by commercial industry wanting to reduce their risk. The impediment to this conversion is capital funding and the fact that it would be harder to bring up palladium lines than it was to eliminate lead from the chemistry. However, there may be a domino effect here similar to the one in which lead was removed in the first place.

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APPENDIX A: ACRONYMS AND ABBREVIATIONS

BMPCOE	Best Manufacturing Center of Excellence
CALCE	Computer Aided Life Cycle Engineering
CERDIP	Ceramic Dual In-Line Package
CTE	Coefficient of Thermal Expansion
CWE	Collaborative Work Environment
DPA	Destructive Physical Analysis
ESPC	Electronics Products and Systems Center
IMC	Intermetallic Compounds
LCC	Leaded Chip Carrier
MDA	Missile Defense Agency
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSL	Moisture Sensitivity Level
ONR	Office of Naval Research
PCB	Printed Circuit Board
PCN	Product Change Notice
PDIP	Plastic Dual Inline Package
PEM	Plastic encapsulated Microcircuits
PLCC	Plastic Leaded Chip Carrier
PN	Part Number
PQFP	Plastic Quad Flat Packs
QFN	Quad Flat No Lead
QFP	Quad Flat Pack
RMS	Raytheon Missile Systems
RMS	Raytheon Missile System
SAM	Scanning Acoustic Microscope
SEM-EDS	Scanning Electron Microscopy with X-ray microanalysis
SM-3	Standard Missile 3
SOD	Small Outline Diode
SOIC	Small Outline Plastic Packages
SOP	Small Outline Packages

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SOT	Small Outline Transistor/Diode
TMTI	Transformational Manufacturing Technology Initiative
TO	Transistor Outline
TQFP	Thin Quad Flat Pack
TSSOP	Thin Shrink Small Outline Package
TWG	Tin Whisker Group
XRF	X-Ray Fluorescence

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